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Research Article

Design of New Multilevel Inverter Topology for Various Unipolar Triangular Carrier PWM Strategies

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Abstract

Multilevel inverters have been widely used for high power and high voltage applications as their performance is highly superior to that of conventional two level inverters due to reduced harmonic distortion, lower electromagnetic interference, and higher dc link voltages but it has some disadvantages such as increased number of components, complex pulse width modulation control method and voltage-balancing problem. In order to compensate the above described disadvantages a new topology with a reversing voltage component is proposed to improve the multilevel performance. This topology requires fewer components compared to existing inverters (particularly in higher levels) and requires fewer carrier signals and gate drives. Therefore, the overall cost and complexity are greatly reduced particularly for higher output voltage levels. Finally, a power circuit of the seven-level proposed topology is developed and simulated with different modulation strategies to show the performance of the inverter by simulation results using MATLAB-SIMULINK. By comparing the various Unipolar Pulse Width Modulation (UPWM) techniques, it is observed that UPDPWM provides less THD and UCOPWM techniques provide higher fundamental RMS output voltage. Compared to the conventional MLI's like DCMLI, FCMLI and CMLI the proposed topology will reduce the number of switches, clamping diodes and clamping capacitors. The proposed topology will have the advantages if the number of levels is increased. The total harmonic distortion will be within IEEE standards. The main object of the proposed topology is to reduce the number of switches compared to conventional MLI's and to achieve the THD within IEEE standards without any additional filter.

Keywords: UCOPWM; UPDPWM; UAPODPWM; UVFPWM; THD; FF; CF; DF

1. Introduction

Multilevel inverter is an array of power semiconductor switches and voltage sources which is switched in a manner that an output voltage of stepped waveform is generated. MLI divide the main

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DC supply voltage into several DC sources which are used to synthesize an AC voltage from a stepped approximation of the desired sinusoidal waveform. The stepped approximation is also popularly known as the staircase model. Traditional two-level voltage source inverter normally produces output voltage with zero (or) positive and negative voltage levels. It suffers from many disadvantages while operating at high frequency mainly due to losses and device ratings of semiconductor switches. To obtain the quality output with less distortion at high switching frequency, multilevel inverters with various PWM strategies are introduced and comparisons are made to choose the better strategy. The general concept involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps. There are several advantages to this approach when compared with the conventional power conversion approach. The smaller voltage steps lead to the production of higher power quality waveforms and also reduced voltage (dv/dt) stress on the load and the electromagnetic compatibility concerns. One of the biggest advantages of using a MLI is that the transformer can be eliminated and this helps to enhance efficiency and cost effectiveness. Additional features such as its battery management capability, redundant switching states in inverter operation, and scalability makes the MLI a suitable choice. Adam et al. (2014) described a quasi two level and three level operation of a diode clamped multilevel inverter using space vector modulation. Ajami et al. (2014) developed a cascade multi-cell multilevel converter with reduced number of switches. Arab Tehrani et al. (2008) proposed a novel multilevel inverter model. Arif et al. (2009) found a new multilevel inverter topology with reduced number of switches. Babaei et al. (2014) proposed extended multilevel converters: an attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters. Domingo Ruiz Caballero et al. (2009) presented a survey on new asymmetrical hybrid multilevel voltage inverter. Ehsan Najafi and Yatim (2012) evaluated the performance of design and implementation of a new multilevel inverter topology. Georgious et al (2010) carried out survey on harmonic elimination control of a five-level DC-AC cascaded H-bridge inverter. Gerardo Ceglia et al. (2004) made a survey on new multilevel inverter topology. Javier Chavarría et al. (2013) proposed a energy balance control of PV cascaded multilevel grid connected inverters under level shifted and phase shifted PWMs. Juan Dixon et al. (2010) performed a asymmetrical multilevel inverter for traction drives using only one DC. Lakshmi Ganesh and Chandra Rao (2012) made a study on Performance of symmetrical and asymmetrical multilevel inverters. Lee and Lee (2014) discussed an open-switch fault detection method and tolerance controls based on SVM in a grid-connected t-type rectifier with unity power factor. Nasrudin Abd. Rahim et al. (2011) found a Performance of symmetrical and asymmetrical multilevel inverters. Palanivel et al. (2014) made a analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques. Rokan Ali Ahmed et al. (2010) developed New Multilevel Inverter Topology with Reduced Number of Switches.

2. Multilevel Inverter

Multilevel inverters have received more attention in industrial applications, such as motor Drives, static VAR compensator and renewable energy systems. Multilevel voltage source inverters are used to increase the number of voltage levels, power rating and allows them to reach higher fundamental RMS voltage with relatively low harmonics without the use of transformers. It has also been shown that a multilevel inverter featuring fault tolerance will have a significantly greater reliability, greater than that of a conventional two-level inverter. The increase in number of voltage levels will significantly lead to decrease in harmonic content and avoids the need of filters and no

EMI problem exists. In this paper, total harmonic distortion (THD) minimization of the output voltage of multilevel inverters is discussed. An efficient approach in reducing the harmonic contents of the inverter's output voltage is THD minimization. In conventional multilevel inverters, the power semiconductor switches are combined to produce a high frequency waveform in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology which reduces the number of carriers and switches used in conventional methods. This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named level generation part and is responsible for generating required level in positive polarity. The switches in this part should have high switching frequency capability. The other part is called polarity generation part and is responsible for generating the polarity of the output voltage, which is the low frequency part operating at line frequency.

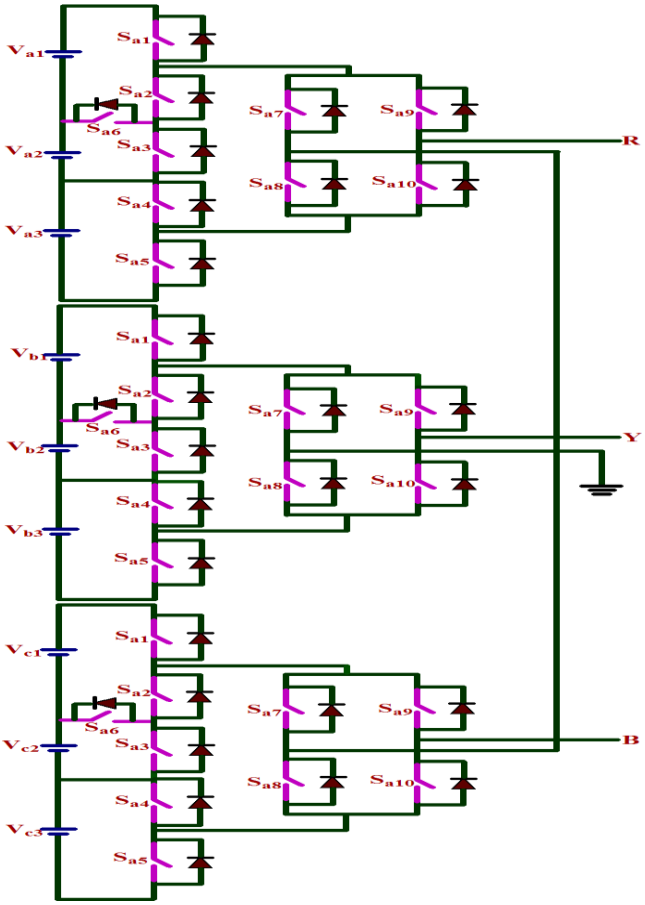

Fig. 1. Three Phase Seven Level Inverter

The topology combines the two parts to generate the multilevel voltage output. In order to generate a complete multilevel output, the positive levels are generated by the high frequency part also named as level generation part, and then, this part is fed to a full-bridge inverter which operates as a polarity generator, which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels

in positive and negative polarities. The topology in seven levels is shown in Fig. 1. As can be seen, it requires ten switches and three isolated sources for single phase. The principal idea of this topology as a multilevel inverter is that the left stage in Fig. 1 generates the required output levels, without negative polarity and the right circuit which is the full-bridge converter decides about the polarity of the output voltage. This part, which is named polarity generator, transfers the required level to the output with the same direction or opposite direction according to the required output polarity. It reverses the voltage direction when the voltage polarity requires to be changed for negative polarity. The middle stage can be duplicated for any number of higher levels so as to get the lesser THD in output voltage. In order to reduce the THD further we go for twenty-five level inverter which can be obtained by further duplicating the middle stage of seven-level inverter. The main advantage of using this twenty-five level inverter is that it needs only 28 switches in single phase where as it is 48 in case of conventional case and it needs only half of the PWM controller compared to conventional inverter. By using this twenty-five level inverter THD can be reduced as per the IEEE standard.

3. Modulation Strategies

In this paper sinusoidal reference, with triangular carriers in unipolar method are chosen to produce the desired output. The function of any inverter is to change a DC input voltage to a symmetric AC output voltage of desired magnitude and frequency which is achieved by various modulation strategies. The number of triangular carriers needed for m level inverter is m-1 for controlling the output voltage, but for unipolar method only m-1/2 carriers are needed. The main advantage of this scheme is half of the carriers are reduced. Four different modulation strategies are introduced in order to increase the output voltage and also to reduce the THD in which the fixed DC is converted into continuous AC signal efficiently by controlling the on and off time of PWM signal. It is generally recognized that, increasing the switching frequency of the PWM pattern results in reducing lower order harmonics. The four different modulation strategies are simulated in this work and the comparisons are made among them to choose the better technique which will be efficient and provides the output with improved power quality. We present the four different PWM techniques such as Unipolar Phase Disposition (UPD), Unipolar Alternate Phase Opposition Disposition (UAPOD), Unipolar Variable Frequency (UVF) and Unipolar Carrier Overlapping Pulse Width Modulation (UCOPWM) schemes. Analysis is carried out to choose the better strategy for the new topology.

3.1 UPDPWM Strategy

In this method all carriers are have the same frequency, same amplitude and same phase (Fig. 2). Carriers needed for twenty-five level inverters is m-1 in conventional strategies, but here we present[(m-1)/2] twelve triangular carriers with one sine reference for the twenty-five level inverter is needed as the chosen topology is a unipolar PWM which consequently will reduce the number of switches as we go for any number of higher levels. All carriers selected above and below the zero reference are in same phase and amplitude of each carrier chosen as 1. Since all carriers are in same phase it is named as Phase Disposition PWM (PDPWM). Amplitude Modulation for this strategy is defined as: Where n is the number of carriers used to generate seven levels.

$$m_a = \frac{A_m}{n * A_c}$$

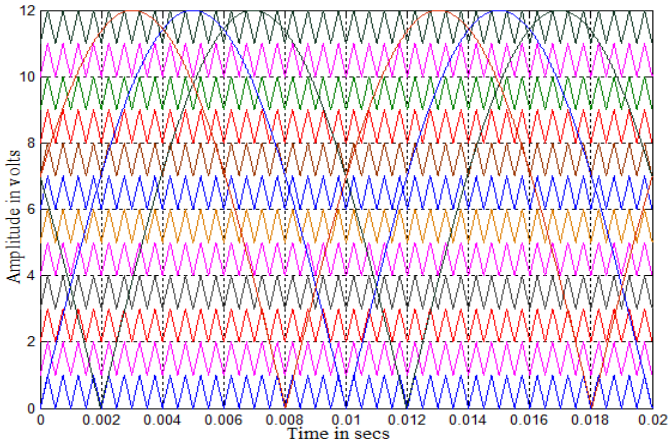

Fig. 2. Modulating and carrier waveforms for UPDPWM strategy (m_a = 1 and m_f = 40)

3.2 UAPODPWM Strategy

In this strategy, carriers are seem to be invert their phase in turns from previous one so it is named as Alternate Phase Opposition Disposition PWM (APODPWM) strategy. Carrier arrangement for this strategy is shown in Fig.3. Carrier set placed above the zero reference with Amplitude Modulation index for this strategy is defined as:

$$m_a = \frac{A_m}{n * A_c}$$

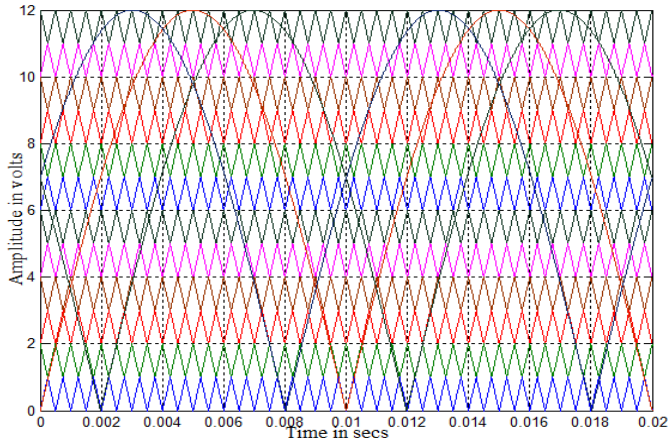

Fig. 3. Modulating and carrier waveforms for UAPODPWM strategy (m_a = 1 and m_f = 40)

3.3 UVFPWM Strategy

Switching pattern is not equal in PDPWM strategy, so to balance the fluctuations in switching pattern for all the switches, variable frequency PWM scheme is used as illustrated in Fig.4. In which

carrier frequency of the intermediate switches is properly increased to balance the number of switching for all the switches. All carriers are in same phase, same amplitude and varying frequency. Hence it is named as Variable Frequency PWM (VFPWM) strategy. Amplitude Modulation index for this strategy is defined as:

$$m_a = \frac{A_m}{n * A_c}$$

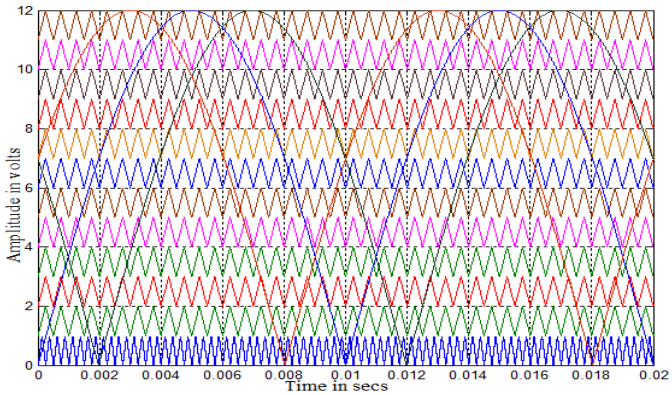

Fig. 4. Modulating and carrier waveforms for UVFPWM strategy (m_a = 1 and m_f = 40 for upper switches and m_a = 1 and m_f = 80 for intermediate switches)

3.4 UCOPWM Strategy

In this method all carriers have the same frequency, same phase and amplitude of each carrier chosen as 1.6 and overlapping amplitude will be 0.8(Ac/2), where A_c is overlapping amplitude of the carrier. Carrier arrangement for this pattern is shown in Fig.5. Amplitude Modulation for this UCOPWM scheme is defined as:

$$m_a = \frac{A_m}{(n-1) * A_c}$$

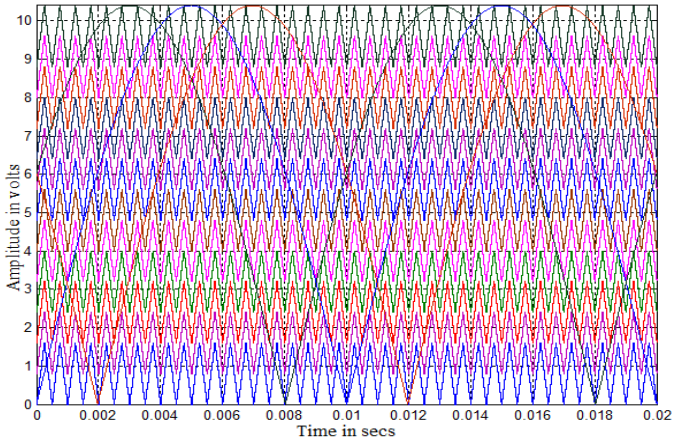

Fig. 5. Modulating and carrier waveforms for UCOPWM strategy (m_a = 1 and m_f = 40)

4. Simulation Results

Simulation studies are performed by using MATLAB SIMULINK to verify the proposed PWM strategies for chosen three phase twenty-five level inverter for various values of m_a ranging from 0.6–1 and corresponding %THD values are measured using FFT plot and they are shown in Table 1. Table 2 shows the V_{RMS} (fundamental) output of inverter for the same modulation indices. Table 3 shows the form factor for different modulation indices which are calculated using RMS voltage and DC component from FFT plots. Table 4 shows crest factor values which are measured using peak voltage and RMS voltage from FFT plots. Table.5 shows the distortion factor for different modulation indices. Figs. 6-13 show the simulated output voltages of chosen twenty-five level inverter and the corresponding FFT plots with different strategies but only for one sample value of m_a = 1 and m_f =40. Fig.6 shows the twenty-five level output voltage generated by UPDPWM strategy and its FFT plot is shown in Fig. 10. Fig.7 shows the twenty-five output voltage generated by UAPODPWM strategy and from of Fig. 11. Fig. 8 shows the twenty-five output voltage generated by UVFPWM strategy and its FFT plot is shown in Fig.11. Fig. 9 shows the twenty-five output voltage generated by UCOPWM strategy and its FFT plot is shown in Fig.13. It is recognised from the overall analysis that the lower order harmonics are eliminated as we go for higher number of levels. The following parameters are used for the simulation results V_{dc}=100V, f_c=2000Hz, f_m=50Hz and R=100Ω.

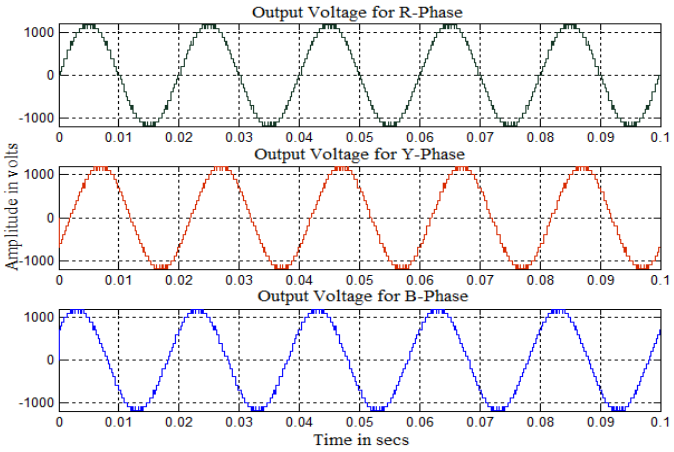

Fig. 6. Simulated output voltage generated by UPDPWM technique for R-load

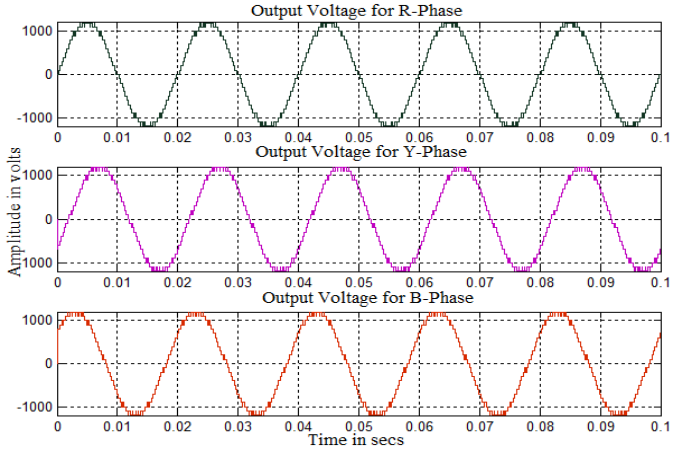

Fig. 7. Simulated output voltage generated by UAPODPWM technique for R-load

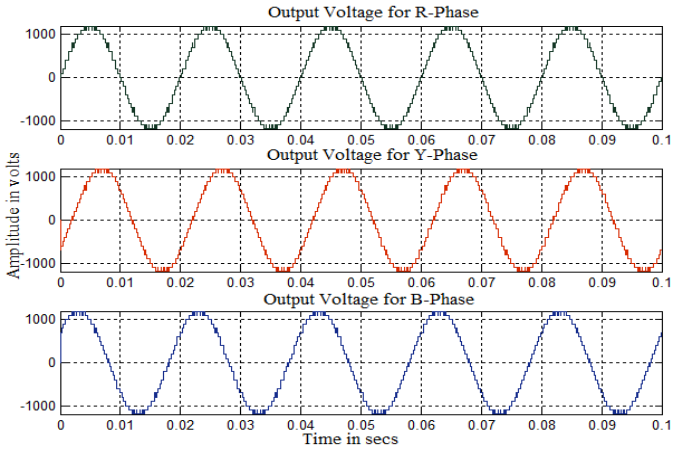

Fig. 8. Simulated output voltage generated by UVFPWM technique for R-load

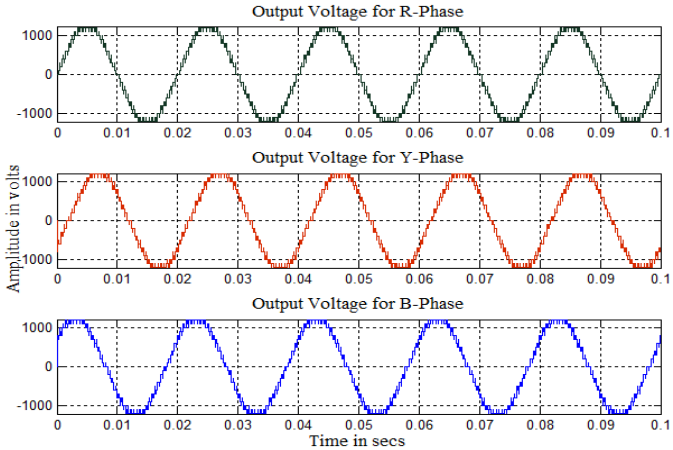

Fig. 9. Simulated output voltage generated by UCOPWM technique for R-load

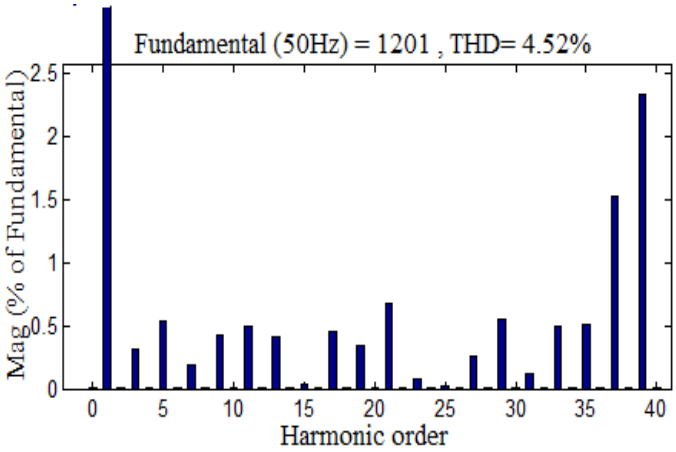

Fig. 10. FFT spectrum for UPDPWM technique

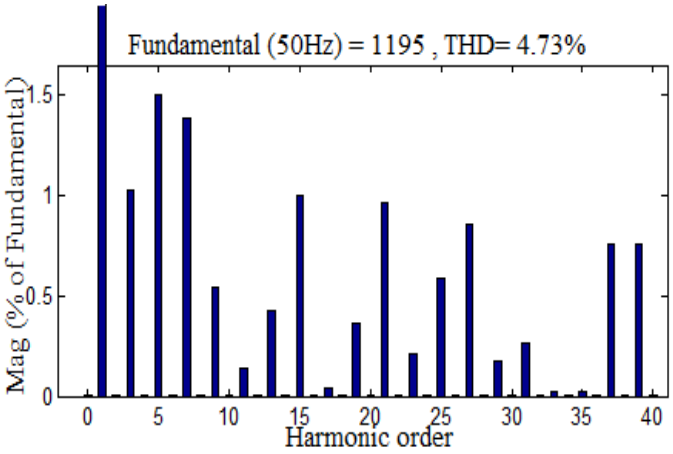

Fig. 11. FFT spectrum for UAPODPWM technique

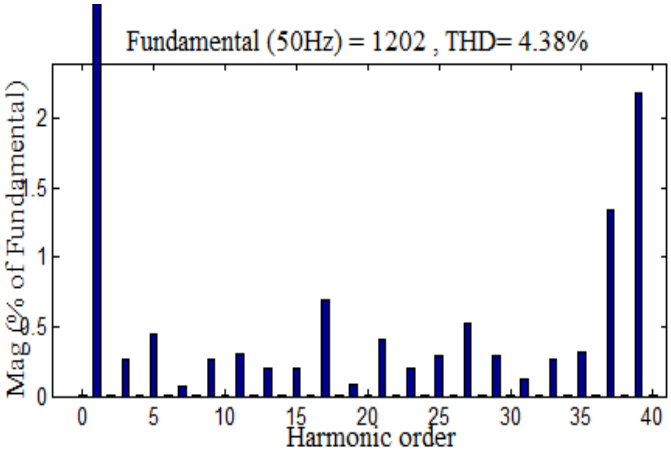

Fig. 12. FFT spectrum for UVFPWM technique

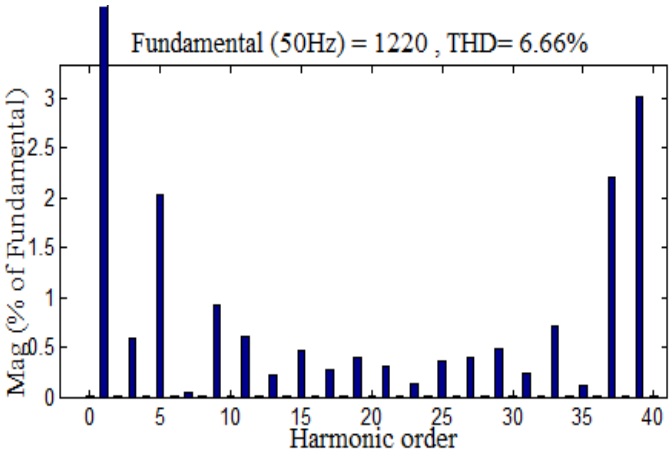

Fig. 13. FFT spectrum for UCOPWM technique

Table 1 % THD of output voltage of chosen MLI for various values of modulating indices

%THD	m_a				
	1	0.9	0.8	0.7	0.6
UPDPWM	4.52	4.99	5.63	6.22	8.82
UAPODPWM	4.73	5.36	6.08	6.66	7.91
UVFPWM	4.38	4.84	5.50	6.10	8.90
UCOPWM	6.66	8.60	9.70	10.84	12.68

Table 2 VRms (Fundamental) of output voltage of chosen MLI for various values of modulating indices

V_{RMS}	m_a				
	1	0.9	0.8	0.7	0.6
UPDPWM	849.5	767.1	680.1	591.6	508
UAPODPWM	845.3	763.5	679.2	594.2	509.1
UVFPWM	849.6	767.2	680.3	591.9	508.1
UCOPWM	862.9	783	691	599.1	508.1

Table 3 Form factor of output voltage of chosen MLI for various values of modulating indices

FF	m_a				
	1	0.9	0.8	0.7	0.6
UPDPWM	INF	INF	INF	INF	INF
UAPODPWM	INF	INF	INF	INF	INF
UVFPWM	INF	INF	INF	INF	INF
UCOPWM	INF	INF	INF	INF	INF

Table 4 Crest factor of output voltage of chosen MLI for various values of modulating indices

CF	m_a				
	1	0.9	0.8	0.7	0.6
UPDPWM	1.4137	1.4144	1.4142	1.4143	1.4141
UAPODPWM	1.4136	1.4145	1.4141	1.4143	1.4142
UVFPWM	1.4147	1.4142	1.4142	1.4140	1.4142
UCOPWM	1.4138	1.4137	1.4141	1.4142	1.4140

Table 5 distortion factor of output voltage of chosen MLI for various values of modulating indices

DF	m_a				
	1	0.9	0.8	0.7	0.6
UPDPWM	0.0425	0.0212	0.0199	0.0391	0.0564
UAPODPWM	0.1315	0.0478	0.0184	0.0148	0.0126
UVFPWM	0.0345	0.0238	0.027	0.0395	0.0501
UCOPWM	0.105	0.208	0.229	0.252	0.275

5. Conclusion

In this paper various new schemes adopting the constant switching frequency and also variable switching frequency multicarrier control freedom degree combination concepts are developed and simulated for the chosen three phase MLI. Performance indices like %THD, V_{RMS} (indicating the amount of DC bus utilization), CF, FF and DF related to power quality issues have been evaluated, presented and analyzed**.** Tables 1 and 2 show the THD and V_{RMS} respectively. Table 3 presents FF for all modulating indices. Tables 4 and 5 display CF and DF for all chosen modulating indices. The result analysis indicate that appropriate UPWM strategies have to be employed depending on the performance measure required in a particular application of MLI based on the criteria of output voltage quality (Peak value of the fundamental, THD and dominant harmonic

components). Among the various unipolar PWM strategies it is inferred that UPDPWM provides better performance with lesser THD. The proposed topology which is applicable for any number of higher levels with less THD and without the use of transformer and filter can be implemented in industrial applications such as AC Power conditioners, static VAR compensators, drive systems, etc and in power generation industries.

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